115 dB SNR Noise Shaping ADC with 50 MHz Bandwidth

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ABSTRACT

This paper presents cascade of integrator with multiple feedforward (CIFF) 7th order 4-bit quantizer delta-sigma modulator. It can achieve 115dB signal-to-noise ratio (SNR) for 50 MHz signal bandwidth with modulator full-scale is 650mV and 5.5 out-of-band-gain (OBG). The signal transfer function (STF) shows a low-pass behavior. The noise transfer function (NTF) of modulator shows high pass filter. The NTF zeroes of the set at DC on the unit circle for maximum quantization noise suppression. The NTF's poles are positioned within the unit circle. The modulator SNR without NTF zero optimization technique is 93 dB, while with NTF zero-optimization technique is 115 dB. The NTF zero optimization techniques shifts these zeroes at the DC and suppresses quantization noise in the signal band. The loop filter optimized for higher performance by integrator performance. The operational amplifiers optimize for DC gain, slew-rate, gain bandwidth product. The thermal noise as well as flicker noise causes the degraded performance. To estimate modulator performance, all circuit non-idealities are modelled. It requires a multi-bit digital-to-analog converter due to the multi-bit quantizer (DAC). To avoid circuit performance degradation, mismatch must be considered. The modulator with 7th order having 4-bit quantizer can achieves SNR of 93 dB with oversampling ratio (OSR) of 12 having sampling frequency 1.2 GHz.

Keywords: Noise shaping, Slew-Rate, DC gain, Noise Transfer Function, Operational amplifier

1. INTRODUCTION

like thermal noise, flicker noise, and finite DC gain of operational amplifier complete A CIFF 7th order modulator is modeled and simulated for signal bandwidth of 50 MHz with OSR of 12 having sampling frequency of 1.2 GHz. The circuit non-idealities modulator model also simulated. A continuous-time modulator having two stages with a quantizer based on a voltage-controlled oscillator is proposed. Through dual path cancellation, the suggested modulator achieves high linearity by suppressing VCOQ voltage-to-frequency nonlinearity. Additionally, because of gain mismatches between the two stages, this architecture is highly resistive to quantization error which is leaking from the first stage to the output. The prototype modulator is built in 65 nm CMOS based technology and has sampling frequency of 1.5 GS/s in a 50 MHz bandwidth, 76.1 dB SNR, 73.5 dB SNDR, 88 dB SFDR and 76.1 dB dynamic range(DR). For a gain mismatch of 10% between the two stages, the prototype provides reliable performance with less than 1.5 dB variation in SNDR. Furthermore, SNDR variance remained within 1 decibel across a 0°C to 80°C temperature range. The modulator power consumption is 51.8 mW with a Walden FOM of 134 fJ/conv-step. [1]. Another wideband modulator is designed for 50 MHz bandwidth. This paper explains a continuous time third order ΔΣ modulator having internal quantizer of four bit sampling at 1GHz with oversampling ratio 10. Because at low oversampling dynamic element

matching is unsuccessful and hard to perform within the loop at large sampling rates, a DAC (digital domain) linearization may be applied to adjust DAC1 non-linearities. Within a 50MHz bandwidth, the proposed modulator achieves an SNDR of 61.7 dB, a DR of 67 dB, and an SFDR of 72 dB in a 1.2V, 90nm CMOS process. Overall, 207 fJ/conv figure of merit has achieved by the modulator. [2]. Another work on wideband modulator. A noise-shaping continuous-time ΔΣ (CTM) based on multistage with on-chip RC time constant calibration circuits, many feedforward interstage paths, and a fully integrated noise-cancellation filter (NCF) is proposed in this paper. A cascade of two single loop second order CTΔΣ modulator stages, active-RC loop filter integrator-based, DACs based on current-steering feedback, and a quantizer which is 4-bit flash, forms the core modulator architecture. To reduce quantization leakage noise owing to variation of process, RC time constant on-chip calibration circuits and multistage operational amplifiers of high-gain are implemented. To: 1) synthesized NTF with dc zeros and fourth order; 2) NCF design simplification; 3) second-stage integrator outputs signal swings minimization, many feedforward interstage paths are introduced. The parameters achieved by prototype chip include SNDR of 74.4 dB, SNR of 75.8 dB, and DR of 76.8 dB in bandwidth (BW) of 50.3 MHz at 1 GHz sampling frequency with power consumption of 43 mW and power supplies from 1.1/1.15/2.5-V, when fully integrated in 40-nm CMOS. It has minimum out-of-band signal transfer function peak and does not need more software calibration. The figure-of-merit (FOM) given is 165.1 dB [3], expressed as

[FOM = SNDR + 10 log 10 (BW/P)]. The proposed work presents a sigma delta ADC which is continuous time for bandwidth of 50 MHz with resolution of 80 dB. It overcomes the known architectures shortcomings and includes a flash ADC of 5 bit as a quantizer with current steering feedback DAC having dynamic element matching. To compensate for excess loop, delay main feedback path & fast feedback path around the quantizer have shifted delays. The model is based on 28 nm FD-SOI technology with forward body bias switched well transistors. At 1.0 V supply voltage, power consumption predicted is 24 mW, and state-of-the-art Schreier FoM is 173 dB [4] after circuit simulations. Because of the requirement of oversampling ratio, clock rate limited the ΔΣ modulator bandwidth. Due to rapid development and progress in nanoscale CMOS technology, now it is possible to design continuous time ΔΣ modulators of wide bandwidth for high frequency applications having high dynamic range. This paper presents 4-bit continuous-time ΔΣ modulator of third order with a single-loop feedforward topology. This modulator is constructed in 40-nm CMOS based process and achieves dynamic range of 80-dB and 100-MHz bandwidth at 2.4 GH clock rate. From 1.2V power supply, modulator consumes 69.7 mW [5].

This paper proposed seven order 4-bit quantizer ΔΣ modulator with 115 dB SNR for 50 MHz signal bandwidth. Out-of-band gain (OBG) of modulator is 5.5 with 650mV of full-scale. The signal-transfer function (STF) behaves as a low-pass whereas the noise-transfer function (NTF) behaves as a high pass filter. To have maximum quantization noise suppression, the NTF zeroes the set at DC on the unit circle. The NTF's poles are placed within the unit circle. The modulator SNR without NTF zero optimization technique is 93 dB, while with NTF zero-optimization technique is 115 dB. These zeroes are

shifted at the DC using NTF zero optimization techniques, quantization noise is suppressed in the signal band. The loop filter optimized for higher performance by integrator performance. The operational amplifiers optimize for DC gain, slew-rate, gain bandwidth product. The thermal noise as well as flicker noise causes the degraded performance.

After the introduction, the second section discuss the design of the modulator design with CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for CT design implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A higher order with seven integrators in the loop filter and four-bit quantizer modulator modeled using Delta-Sigma Toolbox [12]. With the NTF zero optimization technique, cascade of integrator with multiple feedforward (CIFF) was modelled and simulated with a higher OBG of 5.5 with an oversampling ratio of 12. The modulator with CIFF topology can achieve SNR of 115 dB with OSR of 12 for signal band of 50 MHz Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed seven order multiple bit CIFF obtained from Delta-Sigma Toolbox. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [13]. Then these converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero. Figure 1 gives the STF and NTF of the modulator. As it is shown from the Figure 1 clearly that the OBG of the CIFF modulator is 5.5. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal STF and NTF plot for the seventh order modulator proposed is shown by figure 2 and output power spectral density (PSD) plot with 115 dB SNR, achieving effective number of bit (ENOB) of 18-bit is shown in figure 3. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loop filter is assumed having infinite DC gain. The noise floor is at the level of -150dB, the quantization noise is suppressed maximum with seven integrators inside the loop filter. Due to OSR of 12, the signal bandwidth 50MHz. Due to CIFF topology of the modulator the signal swing inside the loop filter is small as a results operational amplifier with very moderate to low DC gain will be utilized for the suppression of the quantization noise. Due to CIFF

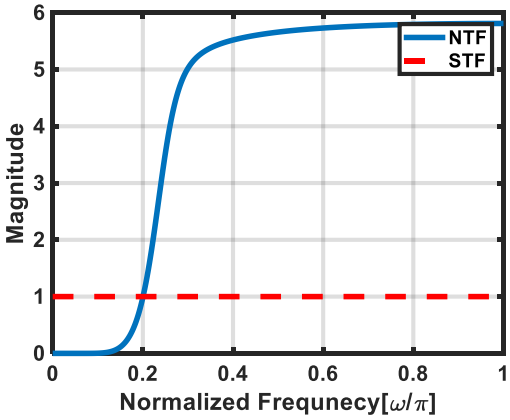

Figure 1: STF and NTF plot (CIFF)

topology the signal swing inside the loop filter is small so that results quite low power operational amplifier for loop filter, while the overall modulator becomes low power. Figure 4 shows the output states of each integrators.

3. RESULTS & DICUSSION

A noise shaping ADC for signal bandwidth of 50 MHz signal bandwidth designed. The loop filter implements CIFF topology in MATLAB. The modulator can achieve SNR of 115 dB with NTF zero optimization technique. The simulation environment SD Toolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A seventh order modulator with multi-bit quantizer modeled and simulation can achieve higher SNR of 115 dB. Non-idealities of operational amplifier circuit like limited DC gain, slew-rate and gain bandwidth investigated. NTF poles lies inside the unit circle. SNR of modulator without NTF zero optimization technique is 93 dB, while with NTF zero-optimization technique is 115 dB. The NTF zero optimization techniques shifts these zeroes at the DC and suppress the quantization noise in signal band. The loop filter optimized for higher performance by integrator performance. The operational amplifiers optimize for DC gain, slew-rate, gain bandwidth product. Thermal noise as well as flicker noise causes the degraded performance. All circuit non-idealities are modeled to estimate the performance of the modulator. It requires a multi-bit digital-to-analog converter due to the multi-bit quantizer (DAC). To avoid circuit

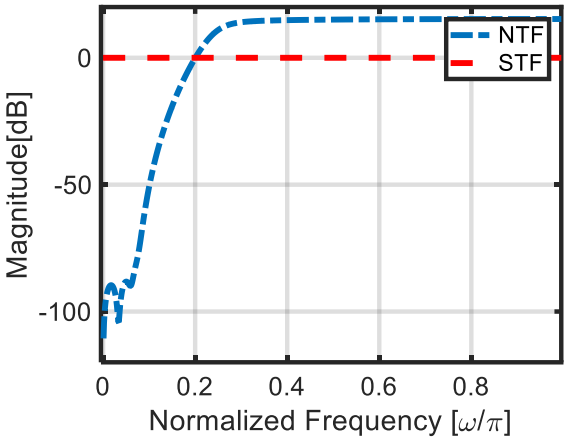

Figure 2: STF and NTF plot (CIFF)

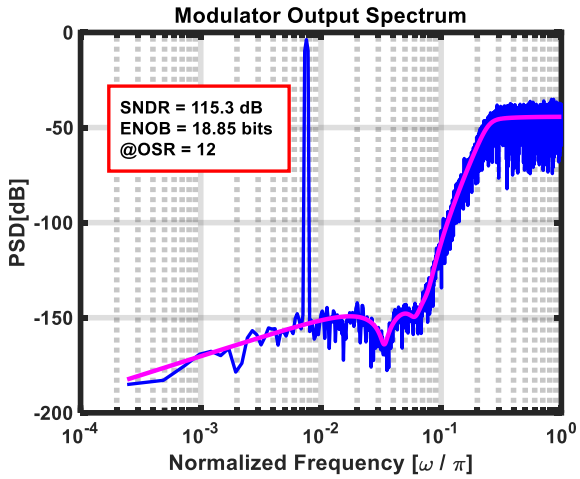

Figure 3: Output power spectral density plot (CIFF)

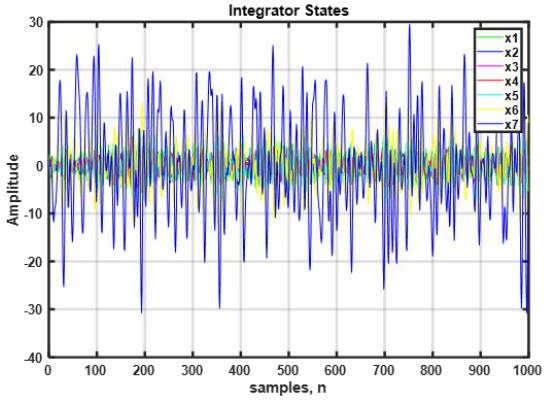

Figure 4: Output states of the integrators

performance degradation, mismatch must be considered. The modulator with 7th order having 4-bit quantizer can achieves SNR of 93 dB with oversampling ratio (OSR) of 12 having sampling frequency 1.2 GHz.

5. ACKNOWLEDGMENT

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